**27.10.2011 – Project Meeting with Moshe**

1. The chosen frame size is according to the VESA standard: 640X480 60Hz.
2. The SDRAM (size 2^20X16X4 = wordXbitXbank) contain number of symbols, each symbol the size of 30X20. (If we use resolution 640x480, then we should take numbers like 40x20 or 20x20, for better division.)

The symbols are saved "Mefuchpachim" (מפוצ'פצ'ים), meaning they are saved row after row in the SDRAM.

Each symbol is RGB = 24 pixels (8 bits for each color of the RGB?)

1. All the components in the structure work in the same frequency (133MHz). That includes: FIFOs, SDRAM, RAM and VESA Generator (But not the VESA itself which works at much lower rate.
2. The frame size is 640X480. The frame is divided into number of blocks; each block is the size of a symbol (30X20). The blocks are aligned, meaning they don't "slide" on one another, but fixed in their place. Each block is referred by a coordinate (x,y).
3. The FPGA contains a RAM that saves for each block (x,y) in the frame the following format code:

* Flag bit, that receives one of the values:
* '1' = the block is active in the frame, and the wanted symbol is in the address that follows
* '0' = the block is not active in the frame, it will receive the default values.
* Address of the desired symbol saved in the SDRAM] .

The depth of the RAM is the number of blocks in the video frame. Each row in the RAM represents a specific block in the frame.

1. The GUI:

* Add/Remove
* If adding a symbol then: A list of the optional symbols will be shown, and the user will choose the desired symbol.
* Location: X=\_\_\_ , Y=\_\_\_ (choosing the block).

GENERATE button.

After pushing the GENERATE button, the MATLAB generates a command of the following structure:

Add or remove

Address of the symbol in the SDRAM

row

column

1. The command itself is wrapped with a startbit, stopbit, CRC, and maybe other stuff from Beeri project (but we don't implement the wrapping process).
2. Need to implement a "command decoder".
3. We have 2 lines of FIFOs (each the size of 20 X30 ) to generate the symbols.

Each FIFO saves one symbol to deliver to VESA Generator.

While first line sending Vesa their data, the other is filled by the SDRAM.

After the first line of symbols is pictured, the 2 FIFOs lines switch tasks (toggle).

1. The first filling of the 2 FIFOs lines happens during the "top not active frame" as defined by VESA Standard.

1. We will use the generics in the VESA Generator for timing the video.

To do list:

1. How many FIFOs there are in FPGA cyclone 2?
2. What is the size of the FIFO?

Is it a 30X20 block or 1X600 (1 row)

1. What is the FIFO,RAM,SDRAM rate?
2. How can it be that the SDRAM and the FIFO have the same rate (133MHz) if in each reading from SDRAM we need to fill number of FIFOs ?

**Principle of operation:**

GUI:

Add/Remove: \_\_\_\_\_\_\_\_

Location: X=\_\_, Y=\_\_

Symbol num: \_\_\_\_

GENERATE button

Generating the command + "command decoder"

In VHDL

In MATLAB

RAM:

[0/1 , symbol address in SDRAM] for block (x,y)=(0,0).

[0/1 , symbol address in SDRAM] for block (x,y)=(0,1).

. . .

[0/1 , symbol address in SDRAM] for block (x,y)=(0,3).

[0/1 , symbol address in SDRAM] for block (x,y)=(1,0).

[0/1 , symbol address in SDRAM] for block (x,y)=(1,1).

. . .

[0/1 , symbol address in SDRAM] for block (x,y)=(3,3).

Frame

Block (0,0)

Block (0,1)

Block (3,3)

SDRAM:

. . .

24X600 bit of first symbol , 0 0 0 0 …

24X600 bit of second symbol , 0 0 0 0 …

24X600 bit of last symbol , 0 0 0 0 …

Filling the 2 lines of FIFOs

But in which way